Remarks

Claims 1 and 11-32 are pending in the application, with claim 1, 11, 12, and 27 being the independent claims.

Applicants acknowledge and appreciate that claims 18 and 32 have been deemed allowable if rewritten in independent form, incorporating elements from rejected base claims, and thank the Examiner for due consideration of these claims.

Reconsideration of the remaining claims in the Application, as well as reconsideration of claims 18 and 32 in their present (i.e., dependent) form, is respectfully requested. Based on the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Rejections under 35 U.S.C. § 102(b)

Claims 1, 11, 14, 21-23, and 27-28 stand rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by U.S. Patent 6,337,682 to Hwang (hereinafter "Hwang").

Applicants respectfully traverse the rejection.

Anticipation of a claim by a reference requires that every element of the claim be disclosed in the reference.

> "In other words, for anticipation under 35 U.S.C. 102, the reference must teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present." MPEP 706.02 (V)

As discussed in detail below, Applicants respectfully submit that several elements of the present system and method, as recited in claim 1 and other independent claims of the present application, are not disclosed by Hwang and are not inherent in Hwang, that is, are not present even by implication.

"Convergence Time" Not Disclosed By Hwang

Page 2 of the Office Action recites text from claim 1 of the present application, specifically:

> "wherein the reestablishment of the synchronization between the video clock signal and the master sync signal occurs over a convergence time, wherein the duration of the convergence time is programmable"

The Office Action alleges that this claim element is anticipated by Hwang:

> "On col. 5 lines 18-21, Hwang discloses the micro-controller generating a frequency divisional value corresponding to the present display mode. ... [T]he frequency divisional values for respective display mode are programmed in the micro-controller. Thus, in the device of Hwang, the frequency divisional value is programmable. As shown on figs 1 and 2, Hwang teaches a phase lock loop synchronizing the clock signal CLKI with the horizontal synchronous signal, and as shown on fig. 2, the locking rate of the phase lock loop is determined by the frequency divisional value. Since the locking rate of the phase lock loop is inversely proportional to the locking period of the phase lock loop, the locking period is programmable. Furthermore, since the locking period represents the time period used to lock/synchronize/converge the clock signal with the horizontal synchronous signal, Hwang does teach the duration of the convergence time being programmable."

Applicants most respectfully submit that the characterization of the Hwang reference within the Office Action is erroneous is several respects.

Hwang appears to disclose a system and method to adjust a frequency of a sampling clock signal CLK1 (see for example Hwang, Abstract; Hwang, col. 6, lines 27-34; Hwang, col. 5, lines 40-46). As per the quote above from the Office Action, the Examiner has alleged that: "... as shown on fig. 2, the locking rate of the phase lock loop is determined by the frequency divisional value ...". [The "frequency divisional value" is referred to hereinafter as "FDV"].

Nowhere in FIG. 2 of Hwang, in the discussion associated with FIG. 2 of Hwang, or elsewhere in Hwang is there disclosure of a "duration of the convergence time" (whether it be a convergence time for PLL to achieve a lock, a convergence time required to adjust the frequency of CLK1, etc.). Moreover, there is no disclosure or implication of a duration of a convergence time as it pertains to reestablishment of synchronization of a video clock signal and a master synch signal, as recited in claim 1. Applicants respectfully request that if there is any such text disclosing such an aspect of

Hwang, or any element(s) of the Hwang figures supporting such an allegation, that the Examiner cite such text/figure-elements in a future Office Action.

Applicants have considered that the Examiner may believe it to be inherent in the function of a phase locked loop that the time it takes to adjust the frequency of CLK1 depends on the value of the FDV. Any such conjecture pertaining to a time it takes to adjust the frequency of CLK1 would fall well beyond the technical scope of the Hwang disclosure. Applicants further submit that any such conjecture would represent impermissible hindsight, reading into Hwang elements which (i) are not disclosed as being operative in Hwang, and (ii) which are only suggested in light of the recited claim elements of the present application, given that there is no disclosure or implication in Hwang either of a time it takes to adjust the frequency of CLK1 or the dependence of such an alleged adjustment time on the value of the FDV.

"*Programmable* Convergence Time" Not Disclosed By Hwang

Claim 1 of the present application recites "... wherein the duration of the convergence time is programmable ...". This is supported in the teachings of the present application, for example:

> "An advantage of the present invention is that the convergence time (i.e., how quickly the slave pulse stream can be synchronized to the master pulse stream) can be *programmably adjusted* via rate controller circuit 314. That is, *the amount of time (i.e., in pixel pulses) added to (or removed from) the slave pulse stream during each iteration of the loop will determine how quickly the loop converges and achieves synchronization.*" (paragraph 0045 of the original application, paragraph 0047 of the published application)

The Examiner has alleged that:

> "Hwang discloses the micro-controller generating a [FDV] corresponding to the present display mode [as determined by Hsync] ... [T]he [FDVs] for respective display mode are programmed in the micro-controller. Thus, in the device of Hwang, the frequency divisional value is programmable. ... the locking rate of [PLL 40] is determined by the [FDV]..."

As already discussed above, Applicants submit that the Examiner has provided no basis to conclude that a convergence time, locking rate, or any other rate or time duration of Hwang, is determined by the FDV. However, *assuming arguendo* that the

FDV has some implication for or influence on a convergence time, locking rate, etc., Applicants submit that this is at best an entirely *incidental result*, and does not constitute a system "... wherein the duration of the convergence time is programmable ...".

As noted by the Examiner, Hwang discloses that "... the [FDVs] for respective display mode are programmed in the micro-controller." In other words, Hwang appears to disclose that possible values for the FDVs are designated with respect to desired display modes, not with a view towards affecting any process completion time. Put another way, the Hwang disclosure (read throughout) appears to require that FDV values be chosen towards the goal of ensuring that the output CLK1 achieves the same frequency as the input Hsync signal. The values selected for the FDV are directed towards achieving a desired signal frequency, not towards controlling a convergence time.

Again *assuming arguendo* that the FDV has any implication for or influence on a convergence time, locking rate, or other time duration (as alleged by the Office Action), Applicants can discern no basis in the Hwang disclosure to determine what kind of change in a the time or rate (for example, shorter or longer) would result from a designated value of FDV or from a designated change in the value of FDV.

Applicants therefore submit that any alleged effect of a change in the FDV on a convergence time, locking rate, etc., in Hwang is not disclosed by Hwang, and further that even if such an effect existed, it would be strictly incidental to the system and method of Hwang. Therefore, selecting values for FDV appears not to affect a convergence time, locking rate, etc. at all, and *assuming arguendo* that the FDV affects a convergence time, locking rate, etc., it cannot reasonably be construed as affecting a convergence time, locking rate, etc., in a way which is "programmable".

Applicants therefore submit that, at least in the above cited respects, Hwang does not disclose a system or method "wherein the reestablishment of the synchronization between the video clock signal and the master sync signal occurs over a convergence time, *wherein the duration of the convergence time is programmable*", as recited in claim 1 of the present application.

Other Elements Not Disclosed By Hwang

Applicants respectfully submit that there are additional elements of the present system and method which are recited in claim 1, and which the Office Action alleges to be anticipated by Hwang, but which are in fact not disclosed by Hwang.

For example, the Office Action alleges that Hwang discloses signal synchronization, and specifically alleges (page 4) that Hwang discloses:

> "... wherein in response to the comparison means determining that the video clock signal is no longer synchronized with the master sync signal, the signal generating means reestablishes the synchronization between the video clock signal and the master sync signal; and ..."

... as recited in claim 1 of the present application.

Hwang appears to disclose *setting a frequency* of an output signal (CLK1) to match the frequency indicated by an input signal (Hsync). Hwang further appears to disclose a system and method which sets an initial frequency for output CLK1 based on the input signal Hsync, and then makes any necessary correction to ensure that the frequency of CLK1 actually matches that of Hsync. Applicants submit that setting a first frequency to equal a second frequency is not the same as synchronizing two signals.

The Office Action alleges that Hwang discloses "... a first display device ...", "... a second display device ...", "... a first computer system ...", and a "... second computer system ....". However, Applicants can discern in Hwang, at most, only a first computer system (providing Hsync), and a single display device (the flat panel device). The Examiner has alleged, for example, that the flat panel display device constitutes, or is equivalent to, the "second computer system". Applicants respectfully submit that a display device is not a computer system, even allowing for a microcontroller within the flat panel display (as disclosed by Hwang). Hwang also does not disclose a second display device.

Applicants further submit that other elements recited in claim 1 of the present application are also not disclosed by Hwang. However, Applicants believe the above-cited elements are sufficient to distinguish the present system and method from Hwang, without further elaboration at this time.

Rejection of Claims 1, 14, 21-23, and Objection to Claim 18

As discussed in detail above, Hwang does not disclose each and every element of claim 1 of the present application. Therefore, Hwang does not anticipate claim 1 under 35 U.S.C. § 102(b). Claims 14 and 21-23 depend from claim 1, and therefore are also not anticipated by Hwang for at least the reasons discussed above with respect to claim 1, and further in view of their own respective features. Similarly, claim 18, already allowed by the Examiner if rewritten in independent form, is submitted to be allowable as a dependent claim (depending from claim 1) in view of the above stated arguments.

Applicants therefore respectfully request that the rejections and objections of claims 1, 14, 18, and 21-23 be reconsidered and withdrawn, and that the claims be allowed.

Rejection of Claims 11 and 27-28

Independent claim 11 of the present application recites unique elements of the present system and method. However, Applicants respectfully submit that arguments presented above with respect to independent claim 1 are pertinent to independent claim 11 as well. For example, independent claim 11 recites a "... a programmable rate value ...". At least the arguments presented above concerning a "convergence time" and a "programmable convergence time" are pertinent to the "... programmable rate value ..." of claim 11. Applicants therefore submit that claim 11 is not anticipated by Hwang for at least the same or substantially similar reasons as those discussed above with respect to claim 1.

Independent claim 27 of the present application recites unique elements of the present system and method. However, Applicants respectfully submit that arguments presented above with respect to independent claim 1 are pertinent to independent claim 27 as well. For example, independent claim 27 recites "... wherein the reestablishment of the synchronization between the video clock signal and the master sync signal occurs over a programmable convergence time, such that a speed of the convergence of the video clock signal and the master sync signal is thereby programmably adjustable ...". At least the arguments presented above concerning a "convergence time" and a "programmable convergence time" are pertinent to the recited element "... wherein the

reestablishment of the synchronization between the video clock signal and the master sync signal occurs over a programmable convergence time, such that a speed of the convergence of the video clock signal and the master sync signal is thereby programmably adjustable ..." of claim 27. Applicants therefore submit that claim 27 is not anticipated by Hwang for at least the same or substantially similar reasons as those discussed above with respect to claim 1.

Claim 28 depends from claim 27, and therefore is not anticipated by Hwang for at least the reasons cited above with respect to claim 27, and further in view of its own respective features.

Applicants therefore respectfully request that the rejections of claims 12, 27, and 28 be reconsidered and withdrawn, and that the claims be allowed.

Rejections Under 35 U.S.C. § 103(a)

Claims 12, 13, 15-17, 19, 20, 24-26, and 29-31 stand rejected under 35 U.S.C. § 103(a) as allegedly being obvious over Hwang in view of various elements which are alleged to be elements within the level of ordinary skill in the art.

Applicants respectfully traverse the rejection.

Rejections of Claims 12-13

Applicants note that in rejection claim 12, the Examiner has alleged:

"Hwang does not expressly disclose the first computer system comprising the input/output module processing the image data" (last two lines of page 7 of the Office Action). The Examiner proceeds to allege that this element would have been obvious to one of ordinary skill in the art.

Applicants express some slight puzzlement, as the cited claim element ("...the first computer system comprising the input/output module processing the image data ...") is not an element of claim 12, but perhaps bears a resemblance to language found in other claims in the application. Applicants respectfully suggest that this was a minor error on the part of the Examiner, and that perhaps the Examiner intended to cite some other element of claim 12 as allegedly being obvious.

For purposes of advancing prosecution of the application, Applicants address the substance of the remainder of the Examiner's comments with respect to claim 12. The Examiner has cited numerous other elements of claim 12 which are alleged to be disclosed by Hwang.

Independent claim 12 of the present application recites unique elements of the present system and method. However, applicants respectfully submit that arguments presented above with respect to independent claim 1 are pertinent to independent claim 12 as well. For example, independent claim 12 recites "... a digital rate controller that divides said clock signal by a divisor value to produce said slave pulse stream, said digital rate controller producing said divisor value based on a *programmable rate value* and a comparison of said master pulse stream and said slave pulse stream ...". At least the arguments presented above concerning a "convergence time" and a "programmable convergence time" are pertinent to the recited element of "... a digital rate controller that divides said clock signal by a divisor value to produce said slave pulse stream, said digital rate controller producing said divisor value based on a *programmable rate value* and a comparison of said master pulse stream and said slave pulse stream ..." of claim 12.

Applicants therefore submit that claim 12 is neither anticipated by Hwang nor rendered obvious by Hwang for at least the same or substantially similar reasons as those discussed above with respect to claim 1.

Claim 13 depends from claim 12, and therefore is also not rendered obvious by Hwang for at least the reasons cited above with respect to claim 12, and further in view of it own respective features.

Applicants therefore respectfully request that the rejections of claims 12 and 13 be reconsidered and withdrawn, and that the claims be allowed.

Rejections of Claims 15-17, 19, 20, and 24-26

Claims 15-17, 19, 20, and 24-26 depend from claim 1. As already discussed in detail above, claim 1 is not anticipated by Hwang, nor has the Examiner alleged that claim 1 would be rendered obvious by Hwang in view of elements within the level of ordinary skill in the art. Claims 15-17, 19, 20, and 24-26, which depend from claim 1,

are therefore also not obvious over Hwang in view of elements within the level of ordinary skill in the art for at least for the reasons cited above with respect to claim 1, and further in view of their own respective features.

Applicants therefore respectfully request that the rejections of claims 15-17, 19, 20, and 24-26 be reconsidered and withdrawn, and that the claims be allowed.

Rejections of Claims 29-31, and Objection to Claim 32

Claims 29-31 depend from claim independent claim 27 by way of dependent claim 28. As already discussed in detail above, claims 27 and 28 are not anticipated by Hwang, nor has the Examiner alleged that claims 27 and 28 would be rendered obvious by Hwang in view of elements within the level of ordinary skill in the art. Claims 29-31, which depend from claims 27 and 28, are therefore also not obvious over Hwang in view of elements within the level of ordinary skill in the art for at least for the reasons cited above with respect to claims 27 and 28, and further in view of their own respective features.

Similarly, claim 32, already allowed by the Examiner if rewritten in independent form, is submitted to be allowable as a dependent claim (depending from claim 27 by way of claim 30) in view of the above stated arguments.

Applicants therefore respectfully request that the rejections of claims 29-31, as well as the objection to claim 32, be reconsidered and withdrawn, and that the claims be allowed.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn, and further that claims 1 and 14-32 be moved to allowance.

Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will

expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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